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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,747	01/08/2007	Masaaki Ogino	FUJI:398	3644

37013 7590 07/09/2009

ROSSI, KIMMS & McDOWELL LLP.
20609 Gordon Park Square, Suite 150
Ashburn, VA 20147

EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
07/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/599,747	OGINO ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2006* is/are: a)☒ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/20/06; 08/29/07; 08/30/07; 3/18/08; 4/14/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to filling of the application on January 08, 2007. Claims 1-11 are pending.

Drawings

1. The Drawing is objected to as the Specification mentions and describes the subject matter in Figure 1 to Figure 7. However, Figure 1 and Figure 2 are only provided. Figures 3-7 are not provided. It is noted that this application is a 371 of PCT/JP05/03731, with the WO 2005/101518 publication.

Accordingly, Applicant is required to furnish a drawing under 37 CFR 1.81(c) in reply to the Office action to avoid abandonment. No new matter may be introduced in the required drawing. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Chung (6,548,374).

Chung teaches (at Fig 3D; col 6, lines 35-56) a method for producing a semiconductor device, which has a trench gate structure, being characterized by comprising the step of: forming an oxide film 110 on an inner wall of a trench 109 formed in a semiconductor substrate 100 by a Chemical Vapor Deposition method using a gas comprising dichlorosilane and dinitrogen monoxide as a raw material.

4. Claim 1-3,5,11 are rejected under 35 U.S.C. 102(b) as being anticipated by Ueda (JP-2003069010).

Re claim 1, Ueda teaches (at Figs 2a-2h; computer English translation page 7-9 of 14; paragraphs 0035-0044) a method for producing a semiconductor device, which has a trench gate structure, being characterized by comprising the step of: forming a first oxide film 4 by a Chemical Vapor Deposition method on an inner wall of a trench formed in a semiconductor substrate 1 (Figs 2a-2c; English translation paragraphs 0035-0040); forming a second thermally oxidized film 5 on an interface between the oxide film 4 and the semiconductor substrate 1 by a thermal oxidation method (Figs 2d-2e); and forming a gate insulating film comprising the first oxide film and 4 the second thermally oxidized film 5 in the trench (Fig 2e). Re claim 2, wherein the oxide film 4 is formed by a Chemical Vapor Deposition (English translation paragraphs 39-42) with a reduced pressure, inherently. Re further claims 3, and claim 11 as applied to claim 1, wherein the oxide film 4 is formed by CVD deposition by using a gas comprising dichlorosilane ($SiClH_2$) and dinitrogen monoxide (N2O) as a raw material (English translation paragraphs 39-40). Re claim 5, wherein the first oxide film 4 has a thickness of about one half (50%) of all the thickness of the gate oxide insulating film (English translation page 7 of 14, last 5 lines).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (JP-2003069010) taken with Hwang et la (6,245,605).

Ueda teaches (at Figs 2a-2h; computer English translation page 7-9 of 14; paragraphs 0035-0044) a method for producing a semiconductor device, as applied to claims 1-3,5 above and fully repeated herein. Re claim 4, wherein the oxide film 4 is formed by CVD deposition (English computer translation paragraphs 39-42), wherein dichlorosilane and dinitrogen monoxide as a raw material is employed for forming the oxide film.

Re claim 4, Ueda does not mention about alternate using of monosilane.

However, Hwang teaches (at col 2, line 44 to col 3) CVD depositing a gate insulating film by alternatively employing either monosilane or dichlorosilane, with oxidation reagents of dinitrogen monoxide (N20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the gate insulating film of Ueda by using either monosilane or dichlorosilane, with oxidation reagents of dinitrogen monoxide (N20), as taught by Hwang. This is because these gases are alternative and art recognized equivalent gases for forming a high quality gate insulating film in a reliable manner.

7. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (JP-2003069010) taken with Suzuki et al (5,506,178).

Ueda teaches (at Figs 2a-2h; computer English translation page 7-9 of 14; paragraphs 0035-0044) a method for producing a semiconductor device, as applied to claims 1-3,5 above and fully repeated herein. Re claims 6-8, wherein the thermally oxidized film 5 is formed on an interface between the oxide film 4 and the semiconductor substrate by an oxidation method (English translation paragraphs 41-42) at a temperature of about 800-1000°C.

Re claims 6-8, Ueda does not mention forming the thermally oxide film by using a pyrogenic oxidation method with a reaction gas diluted with an inert gas.

However, Suzuki teaches (at col 4, line 50 to col 5; col 1) forming a thermally oxidized film on a semiconductor substrate by employing a high-temperature-dilution pyrogenic oxidation method which is performed by diluting a reaction gas with an inert gas and is performed with high temperature of about 800-1200°C

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the thermally oxidizied film of Ueda by using a pyrogenic oxidation method with a reaction gas diluted with an inert gas, at high temperature up to 1200°C, as taught by Suzuki. This is because of the desirability to reducing defects incorporated in the region of the semiconductor substrate. The subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of temperature, as taught by Suzuki, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942).

8. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (JP-2003069010) taken with Cheng et al (6,649,538).

Ueda teaches (at Figs 2a-2h; computer English translation page 7-9 of 14; paragraphs 0035-0044) a method for producing a semiconductor device, as applied to claims 1-3,5 above and fully repeated herein.

Re claims 9-10, Ueda teaches forming the gate insulating film, but does not teach performing an annealing treatment in nitrogen (claim 9), and at a temperature of about 850-1000°C.

However, Cheng teaches (at col 7, lines 1-35; col 6, lines 10-50; 4; col 4, lines 2-67; Fig 2) forming the gate insulating film 22, and performing an annealing treating in an atmosphere of nitrogen at a temperature of form about 900-1000°C.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate insulating film of Ueda by further performing an annealing treating in an atmosphere of nitrogen at a temperature of form about 900-1000°C, as taught by Cheng. This is at least because of the desirability to improve electrical properties including leakage current and improved charge mobility of the gate insulating film. The subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was

made to select the portion of the prior art's range of temperature, as taught by Cheng, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-24-7

/Michael Trinh/
Primary Examiner, Art Unit 2822